1. A method of performing bus inversion on first bits to be transmitted on a bus, said method comprising the steps of:

capturing a state of previously transmitted bits on the bus;

capturing a state of an inversion bit associated with the previously transmitted bits; and

determining from the captured state of the previously transmitted bits whether the first bits should be inverted.

2. The method of claim 1 further comprising the step of inverting the first bits if it is determined that the first bits should be inverted.

3. The method of claim 2 further comprising the steps of:

outputting the inverted first bits on the bus; and

outputting the inversion bit with a value indicating that the first bits have been inverted.

4. The method of claim 1 further comprising the steps of:

outputting the first bits on the bus; and

outputting the inversion bit with a value indicating that the first bits have not been inverted.

5. The method of claim 1, wherein said determining step comprises:

obtaining a number of first bits that match the previously transmitted bits;

determining whether the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits; and

setting the inversion bit to a value indicating that the first bits should not be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits.

6. The method of claim 5 further comprising the steps of:

determining whether the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits; and

setting the inversion bit to the captured state of the inversion bit if it is determined that the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits.

7. The method of claim 6, wherein the number of first bits is an even number.

8. The method of claim 6 further comprising the step of setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than or equal to one half the number of first bits.

9. The method of claim 5 further comprising the step of setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than one half the number of first bits.

10. The method of claim 9, wherein the number of first bits is an odd number.

18

11.   The method of claim 1, wherein said capturing steps are performed only when the first bits are available for transfer over the bus.

12.   The method of claim 1, wherein said capturing steps are performed for every transfer on the bus.

13.   The method of claim 1, wherein said determining step is based on reducing a number of transitions of the first bits and the inversion bit.

14.   The method of claim 1, wherein said determining step is based on reducing the number of first bits having a predetermined logical state.

15.   The method of claim 14, wherein the predetermined logical state is a logical one.

16.   The method of claim 14, wherein the predetermined logical state is a logical zero.

17.   A method of outputting first bits on a bus, said method comprising the acts of:

determining from a previous state of the bus and a previous state of an inversion bit associated with the first bits whether the first bits should be inverted;

if it is determined that first bits should be inverted,

outputting inverted first bits on the bus, and

outputting on a separate line the inversion bit with a value indicating that the first bits have been inverted; and

if it is determined that first bits should not be inverted,

outputting the first bits on the bus, and

outputting on a separate line the inversion bit with a value indicating that the first bits have not been inverted.

18.   The method of claim 17, wherein said determining step comprises:

obtaining a number of first bits that match a state of previously transmitted bits;

determining whether the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits; and

setting the inversion bit to a value indicating that the first bits should not be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits.

19.   The method of claim 18 further comprising the steps of:

determining whether the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits; and

setting the inversion bit to a previous state of the inversion bit if it is determined that the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits.

20.   The method of claim 19 further comprising the step of setting the inversion bit to a value indicating that the first bits should be inverted if it is

determined that the obtained number of first bits that match the previously transmitted bits is not greater than or equal to one half the number of first bits.

21.   The method of claim 18 further comprising the step of setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than one half the number of first bits.

22.   The method of claim 17, wherein said determining step is based on reducing a number of transitions of the first bits and the inversion bit.

23.   The method of claim 17, wherein said determining step is based on reducing the number of first bits having a predetermined logical state.

24.   The method of claim 23, wherein the predetermined logical state is a logical one.

25.   The method of claim 23, wherein the predetermined logical state is a logical zero.

26.   A system comprising:

a first device; and

a second device connected to said first device by a first bus and an associated inversion bit line, said first device transmitting first bits over the first bus to the second device by capturing a state of previously transmitted bits on the first bus, capturing a state of an inversion bit on the inversion bit line and determining from the captured state of the previously transmitted bits whether the first bits should be inverted.

27. The system of claim 26, wherein said first device inverts the first bits if it is determined that the first bits should be inverted.

28. The system of claim 27, wherein said first device outputs the inverted first bits on the first bus and outputs the inversion bit on the with a value indicating that the first bits have been inverted.

29. The system of claim 26, wherein said first device outputs the first bits on the first bus and outputs the inversion bit with a value indicating that the first bits have not been inverted.

30. The system of claim 26, wherein said first device determines whether the first bits should be inverted by obtaining a number of first bits that match the previously transmitted bits, determining whether the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits and setting the inversion bit to a value indicating that the first bits should not be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits.

31. The system of claim 30, wherein if said first device determines that the obtained number of first bits that match the previously transmitted bits is not greater than one half the number of first bits, said first device determines whether the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits and sets the inversion bit to the captured state of the inversion bit if it is determined that the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits.

32. The system of claim 31, wherein said first device sets the inversion bit to a value indicating that the first bits should be inverted if it is determined that the

22

obtained number of first bits that match the previously transmitted bits is not greater than or equal to one half the number of first bits.

33. The system of claim 30, wherein said first device sets the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than one half the number of first bits.

34. The system of claim 26, wherein said first device captures the states of the previously transmitted bits and inversion bit only when the first bits are available for transfer over the first bus.

35. The system of claim 26, wherein said first device captures the states of the previously transmitted bits and inversion bit for every transfer on the first bus.

36. The system of claim 26, wherein said first device determines whether to invert the first bits based on reducing a number of transitions of the first bits and the inversion bit.

37. The system of claim 26, wherein said first device determines whether to invert the first bits based on reducing the number of first bits having a predetermined logical state.

38. The system of claim 26, wherein the first bus is an address bus.

39. The system of claim 26, wherein the first bus is a portion of an address bus.

40. The system of claim 26, wherein the first bus in a command bus.

41. The system of claim 26, wherein the first bus is a data bus.

42. The system of claim 26, wherein the first bus is a portion of a data bus.

43. The system of claim 26, wherein a number of first bits comprises four bits.

44. The system of claim 26, wherein a number of first bits comprises eight bits.

45. The system of claim 26, wherein a number of first bits comprises nine bits.

46. The system of claim 26, wherein a number of first bits comprises sixteen bits.

47. The system of claim 26, wherein a number of first bits comprises thirty-two bits.

48. A system comprising:

a first device; and

a second device connected to the first device by a plurality of buses, at least a first bus of said plurality of buses being associated with a first inversion bit line, said first device transmitting first bits over the first bus by determining from a previous state of the first bus and a previous state of an inversion bit on the first inversion bit line whether the first bits should be inverted, if it is determined that first bits should be inverted, outputting inverted first bits on the first bus and outputting the inversion bit with a value indicating that the first bits have been inverted, and if it is determined that first bits should not be inverted, outputting the first bits on the first bus, and outputting the inversion bit with a value indicating that the first bits have not been inverted.

49. The system of claim 48, wherein said first device determines whether to invert the first bits based on reducing a number of transitions of the first bits and the inversion bit.

50.   The system of claim 48, wherein said first device determines whether to invert the first bits based on reducing the number of first bits having a predetermined logical state.

51.   The system of claim 48, wherein the first bus is an address bus.

52.   The system of claim 48, wherein the first bus is a portion of an address bus.

53.   The system of claim 48, wherein the first bus in a command bus.

54.   The system of claim 48, wherein the first bus is a data bus.

55.   The system of claim 48, wherein the first bus is a portion of a data bus.

56.   The system of claim 48, wherein a number of first bits comprises four bits.

57.   The system of claim 48, wherein a number of first bits comprises eight bits.

58.   The system of claim 48, wherein a number of first bits comprises nine bits.

59.   The system of claim 48, wherein a number of first bits comprises sixteen bits.

60.   The system of claim 48, wherein a number of first bits comprises thirty-two bits.

61.   The system of claim 48, wherein a second bus of said plurality of buses is associated with a respective second inversion bit line and said first device transmits second bits over the second bus by determining from a previous state of the second bus and a previous state of a second inversion bit on the second inversion bit line whether the second bits should be inverted, if it is determined that second bits should be

25

inverted, outputting inverted second bits on the second bus and outputting the second inversion bit with a value indicating that the second bits have been inverted, and if it is determined that second bits should not be inverted, outputting the second bits on the second bus, and outputting the second inversion bit with a value indicating that the second bits have not been inverted.

62.   A system comprising:

first, second and third devices connected to each other by a first bus and an associated inversion bit line, said first device transmitting first bits over the first bus to one of the second and third device by capturing a state of previously transmitted bits on the first bus, capturing a state of an inversion bit on the inversion bit line and determining from the captured state of the previously transmitted bits whether the first bits should be inverted.

63.   A system comprising:

means for capturing a state of previously transmitted bits on a bus;

means for capturing a state of an inversion bit associated with the previously transmitted bits;

means for determining from the captured state of the previously transmitted bits whether the first bits should be inverted;

means for transmitting inverted first bits on the bus and an inversion bit having a value indicating that the first bits have been inverted if it has been determined from the captured state of the previously transmitted bits that the first bits should be inverted; and

26

means for transmitting the first bits on the bus and an inversion bit

having a value indicating that the first bits have not been inverted if it has

been determined from the captured state of the bits that the first bits

should not be inverted.